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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/674,682 | ELBOIM ET AL. | |
| | Examiner | Art Unit | |
| | Jesse Diller | 2187 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-4,6-13,15-21,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-13,15-21,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## *Response to Amendment*

1. Examiner acknowledges receipt of the amendment in response to the office action dated 1/31/2007, which amendment was received 04/09/2007. At this point, claims 1 and 20 have been amended. Thus, claims 1-4, 6-13, 15-21, and 24-25 are now pending in the application.

## ***Response to Arguments***

2. **Applicant's arguments filed with respect to the 35 USC § 112 rejections of claims 15 have been fully considered and are persuasive**. The rejection is withdrawn in light of Applicant's remarks.

3. **Applicant's arguments filed with respect to the 35 USC § 102 rejections of claims 1-2 and 6-7 by Kao have been fully considered but are not persuasive**. Applicants contend that Kao does not teach a memory with a maximum memory size less than a size sufficient to fill all registers as claimed in claim 1. However, as noted in the prior Office Action in par. 6, the memory storing configuration information (0-5n in Fig. 5) is sized in multiples of the configuration register size, so as to be sized in accordance with the amount of information to be written. Therefore, when the configuration writes less than all of the registers, the memory storing configuration information has a size less than a size sufficient to fill all the registers.

4. **As for Applicant's arguments on page 8**-9 regarding the definition of "memory design validation test", Applicants attempt to further define the term here. However, the

limitations put forth here (esp. line 5, page 9) are not supported by the specification. Further, were the Applicant's definitions here accepted, a question under 35 USC § 112 would be raised. How can Applicant claim a device which performs functions prior to its manufacturing? Therefore, the "memory design validation test" is taken to "exclude normal operating mode", as before.

5. **Applicant's arguments filed with respect to the 35 USC § 103 rejections of claims 8-10, 11-13, 15-19, 24-25 by Kao, Tomashima, and Bonaccio in various combinations have been fully considered but they are not persuasive.** Applicants argue, as above, the definition of "memory design validation test". The remarks in par. 3 above are incorporated here.

6. Applicants further argue that the motivation for combining the references is improper, because Kao and Bonaccio are related to programming configuration registers, while Tomashima teaches adjusting reference voltages to a memory circuit for skew reduction.

However, as shown in Fig. 43 and Col. 37 of Tomashima, the timing delay is clearly a unit of configuration information. Further, during the initialization of a memory device, various timing settings are tried (i.e., reset and load a value, test, and if the result is unfavorable, S5, Fig. 43, repeat the process with a different timing value). This *incremental process* is used to determine correct configuration settings of a memory device, and clearly would be applicable to more systems than just that of Tomashima. Further, while Bonaccio and Kao teach programming registers from a BIOS, and Tomashima teaches memory voltage control, it is well known that many BIOSes are

able to control the voltage of the memory. Therefore, one of ordinary skill would be motivated to use this cyclic load-test-update process in the system of Kao and Bonaccio, as noted in the prior office action.

7. **Applicant's arguments filed with respect to the 35 USC § 103 rejections of claims 20-21 by Kao, Tomashima, and Bonaccio and Cohen have been fully considered but they are not persuasive.**

8. Applicants argue, as above, the definition of "memory design validation test". The remarks/reply in par. 3 above are incorporated here.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

**1. Claims 1-2, 6-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Kao et al., US 6,119,192.**

**2. As for claim 1, Kao teaches:**

- a non-volatile memory storing information to load a plurality of configuration registers of a device (160, Fig. 1),
- the loading occurs during a memory design validation stage (As noted in Par. 2, page 8 of the reply dated 10/23/06, the 'during a memory design validation stage'

"is only to exclude normal operating mode". The process of Kao happens not in normal operating mode, but during a configuration mode. See Col. 2, lines 42-46), wherein

- the information includes a plurality of address information and a plurality of data corresponding to the plurality of address information (see address information 0, 5, 5m, 5n and data information 1-4, 6, 5m+1-5m+4, Fig. 5),
- each of the plurality of address information identifying at least one of the plurality of configuration registers to which a corresponding data should be written (see Fig. 5; the address information is an index referring to the appropriate register; see 365, Fig. 3).

3. **As for claim 2, Kao additionally teaches:**

- The non-volatile memory is an Electrically Erasable Programmable Read-only Memory (See Col. 3, line 43) and
- the configuration registers are used to define parameters for communication between the device and at least one other device (See Cols 1-2).

4. **As for claim 6, Kao additionally teaches:**

- a block of control logic coupled to the memory, the block of control logic to write the plurality of data to the plurality of configuration registers according to the plurality of address information (see 205, Fig. 2; for multiple logic blocks which control the loading).

5. **As for claim 7, Kao additionally teaches:**

- the plurality of configuration registers are to be loaded during an initialization of the device (Col. 3, lines 27-35: section b; the loading happens on startup).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**6. Claims 3-4, 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao in view of Bonaccia et al., US 2004/0143715.**

7. **As for claims 3-4, Kao teaches** the limitations of claim 1, as above. Kao does not teach, however, that the device is an analog communication device, as does claim 3 or that the device is a processor, memory controller, or Ethernet controller, as does claim 4.

8. Bonaccio teaches a system and method for loading sets of configuration registers from a non-volatile memory. He teaches, in Pars. 4 and 20-21, that many Ics allow the user to configure the circuit using configuration registers. He cites several examples, such as in HD read channel controllers or microprocessors in Par. 4 and analog communications circuits in the last lines of Par. 6. Further, in Pars. 20-21, he teaches that the methods of loading configuration registers may be applied not only to ICs such as hard disk channel controllers, but to any IC configured by registers.

9. Kao and Bonaccio are analogous art,because they are from the same area of endeavor, namely systems for setting configuration registers.

10. At the time of the invention it would have been obvious to use the system of setting configuration registers as taught by Kao in an environment such as a microprocessor or analog communication circuit.

11. The motivation for doing so is taught by Bonaccio in Par. 4, namely that using programmable registers is widely used in many ICs to allow the user to configure the function of the chip. Further, Kao teaches in Col. 3, lines 60-66 that his invention would be beneficially used in many systems where it is desirable to configure a peripheral device in an expedited manner prior to a normal system initialization procedure.

12. Therefore, it would have been obvious to use the register loading process of Kao in different environments, thereby obtaining the invention of claims 3-4.

**13. As for claim 8, Kao teaches:**

- loading the plurality of configuration registers (365, Fig. 3; see also Col. 3, lines 27-35: section b) according to information stored in a non-volatile memory (160, Fig. 1), wherein
- the information in a memory includes a plurality of address information and a plurality of data corresponding to the plurality of address information, each of the plurality of address information identifying at least one of the plurality of to which a corresponding data should be written (see address information 0, 5, 5m, 5n and data information 1-4, 6, 5m+1-5m+4, Fig. 5; see also Fig. 5; the address information is an index referring to the appropriate register; see 365, Fig. 3); and
- the loading occurs during a memory design validation stage (As noted in Par. 2, page 8 of the instant reply, the 'during a memory design validation stage' "is only

to exclude normal operating mode". The process of Kao happens not in normal operating mode, but during a configuration mode. See Col. 2, lines 42-46) .

14. Kao does not teach, however,

- resetting each of a plurality of configuration registers of a device to a register default data value before loading the registers.

15. **Bonaccio teaches** a system and method for loading sets of configuration registers from a non-volatile memory. He teaches, in Par. 6, that configuration values may come from several sources. Usually, the registers are made up of latches which are designed to be reliably reset to a specific state when power is first applied. He also teaches that rather than hard-wiring these values, a POR value memory, 14, Fig. 1, may be used to reset each of the configuration registers to a default value which can be changed and subsequently reset from the non-volatile memory.

16. Kao and Bonaccio are analogous art,because they are from the same area of endeavor, namely systems for setting configuration registers.

17. At the time of the invention it would have been obvious to modify the system of Kao to use the Power-on value memory taught by Bonaccio to reset the registers to a default value on power-up.

18. The motivation for doing so is taught by Bonaccio in Pars 6-7, namely that sometimes the default values are correct, and sometimes they need to be changed. Therefore, it would have been obvious to use the default register value of Bonaccio in the system of Kao, thereby obtaining the system of claim 8.

**19. As for claim 9, Kao also teaches:**

- The loading occurs during the initialization of a communication controller device (see 150-160, Fig. 1 and Fig. 2; the system is a PCI communications bus controller).

**20. As for claim 10, Kao also teaches:**

- updating the information stored in the non-volatile memory with a second plurality of address information and second a plurality of data corresponding to the second plurality of address information, each of the second plurality of address information identifying at least one of the plurality of to which a corresponding one of the second plurality of data should be written (Col. 7, lines 10-25).

**21. Claim 11-13, 15-19, 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bonaccio in view of Kao and Tomashima.**

**22. As for claims 11, 15, Bonaccio discloses:**

- selecting a desired configuration of a device, the desired configuration associated with desired data to be stored in a plurality of registers of the device; (see Par. 9; also Par. 29, first 5 lines; also first half of Par. 27; the start register designates a configuration set)
- storing test information associated with the desired configuration in a memory (Par. 29, Fig. 1; the configuration sets are test information associated with various configurations);
- resetting each of the plurality of registers to a register default data value (Par. 6);
- loading at least two of the plurality of registers according to the test information (Par. 32),

23. Bonaccio does not expressly disclose that

- the test information includes a plurality of test address information and a plurality of test data corresponding to the plurality of test address information, each of the plurality of test address information identifying at least one of the plurality of registers to which a corresponding test data should be written; or

24. Instead, Bonaccio teaches that the configuration sets stored in the non-volatile memory contain only data; an address generator, a start register, and a duration register (144, 150B, 150C, Fig. 2) are used to generate the addresses which correspond to the data and to the target register.

25. Kao discloses a similar system and method of loading configuration registers, where initialization data is stored in a non-volatile memory and subsequently loaded into the registers during system startup. In the system of Kao, an address generator is not used. Instead, the register address is stored in the memory along with the data to =be stored. See Fig. 5.

26. Bonaccio and Kao are analogous art because they are from the same area of endeavor, namely systems for loading configuration registers.

27. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Bonaccio by replacing the address generator and address registers 150b,c with the address+data system of Kao.

28. The motivation for doing so is taught by Kao on Col. 3, lines 9-15, namely that this increases system efficiency and speed. Because the address is already stored in

the memory, the address generator does not need to generate an address; it can simply be loaded with the data.

29. Therefore, it would have been obvious to combine Kao with Bonaccio for the benefit of increased circuit simplicity and speed.

30. Bonaccio also does not expressly teach:

- identifying a subset of the plurality of test data that correspond to a subset of the plurality of registers having default data values equal to desired data for achieving the desired configuration *prior* to loading, and
- that the process is done during a memory design validation stage.

**31. Tomashima teaches** a system for synchronization and setup of memory devices. In this system, several variables are tested, delay and Vref (see Fig. 43). Multiple series of tests are run. Delay and Vref are initialized (to a default value) and the configuration tested (s4). If the test is successful, that is one item of test data having default value equal to desired data. In that case, an additional subset of the test data (Vref) is identified S6 and the test run again with a different value.

32. Tomashima and the system of Kao and Bonaccio are analogous art because they are from the same area of endeavor, namely memory system configuration.

33. At the time of the invention it would have been obvious to one of ordinary skill in the art to utilize the method of Tomashima in the system of Kao and Bonaccio for memory validation. Such a combination, recognizing that certain default values - while operable - are not optimal, would be motivated to retry the reset/loading/identifying

process with different values in order to obtain optimal operation (see Tomashima, Col. 37, lines 25-30).

34. Therefore, it would have been obvious to combine Tomashima and the system of Kao and Bonaccio, thereby obtaining the invention as claimed in claim 11 and 15.

**35. As for claims 24-25, the system of Bonaccio, Kao, and Tomashima further teaches:**

- repeating a multi-stage test data loading process, wherein repeating comprises storing subsequent test information and repeating c), d), and e) using the subsequent test information (note Tomashima, Fig. 43 and the discussion of Par. 35 above).

**36. As for claim 12-13, the system of Bonaccio, Kao, and Tomashima further teaches:**

- wherein the test information includes a word of register address information and corresponding register data words for each one of the plurality of registers (see Fig. 5, Kao; the test information includes a register address and corresponding data; see also Bonaccio, last half of Par. 23).

**37. As for claim 16, the system of Bonaccio, Kao, and Tomashima teaches:**

- resetting and loading occur during initialization of a communication controller device (see Bonaccio, ; Kao, Col. 3, lines 27-35: section b; the loading happens on startup).

**38. As for claim 17, the system of Bonaccio, Kao, and Tomashima teaches:**

- generating a desired information associated with the desired configuration, wherein generating comprises: if there exists at least one of the plurality of test data corresponding to one of the plurality of registers having default data values equal to desired data for achieving the desired configuration prior to loading, then storing subsequent test information and repeating c), d), and e) using the subsequent test information; else identifying the desired information to be the test information. (see Tomashima, s4, s6-s7, Fig. 43. If the default vernier value is the correct one, as determined in step s1-s4 but the Vref is not max, then subsequent Vref values are utilized and the test is rerun (s7). Else, the desired information is set (s8)).

39. **As for claim 18, the system of Bonaccio, Kao, and Tomashima teaches:**

- Selecting a memory with a memory size less than or equal to a memory size sufficient to store the desired information (The memory has a size equal to a memory size sufficient to fill some or all the configuration registers; therefore it has a size equal to a size sufficient to store the information)

40. **As for claim 19, the system of Bonaccio, Kao, and Tomashima teaches:**

- Selecting a desired memory includes reducing a size of the memory to a size sufficient to store the subset of the plurality of these data and the corresponding test address information (see Bonaccio, Fig. 2: the size of the memory is sufficient to store the data).

**41. Claims 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao in view of Bonaccio and Cohen, US 5,737,524.**

**42. Kao teaches**

- a plurality of configuration registers of a device (210, Fig. 1),
- a non-volatile memory storing information to load a plurality of configuration registers of a device (160, Fig. 1), wherein
- the loading occurs during a memory design validation test (As noted in Par. 2, page 8 of the reply dated 10/23/06, the 'during a memory design validation stage' "is only to exclude normal operating mode". The process of Kao happens not in normal operating mode, but during a configuration mode. See Col. 2, lines 42-46), wherein
- the information includes a plurality of address information and a plurality of data corresponding to the plurality of address information (see address information 0, 5, 5m, 5n and data information 1-4, 6, 5m+1-5m+4, Fig. 5),
- each of the plurality of address information identifying at least one of the plurality of configuration registers to which a corresponding data should be written (see Fig. 5; the address information is an index referring to the appropriate register; see 365, Fig. 3).
- a block of control logic coupled to the memory, the block of control logic to write the plurality of data to the plurality of configuration registers according to the plurality of address information (see 205, Fig. 2; for multiple logic blocks which control the loading).

- The non-volatile memory is an Electrically Erasable Programmable Read-only Memory (See Col. 3, line 43) and
- the non-volatile memory has a memory size less than a memory size sufficient to fill all the configuration registers (The memory has a size equal to a memory size sufficient to fill some or all the configuration registers; see Col. 3, lines 10-15 and Claim 2. The memory storing configuration information (0-5n in Fig. 5) is sized in multiples of the configuration register size, so as to be sized in accordance with the amount of information to be written. Therefore, when the configuration writes less than all of the registers, the memory storing configuration information has a size less than a size sufficient to fill all the registers)

43. Kao does not expressly teach that the device is an Ethernet controller device, instead teaching a PCI/ISA bus bridge.

44. Cohen teaches a similar system for loading configuration registers of a PCI/peripheral bus interface (24, Fig. 2) from a non-volatile memory (12D, Fig. 2). Cohen teaches that the PCI bus bridge may be used to interface different devices to the bus, such as an Ethernet device or a SCSI interface (Col. 2, lines 6-10).

45. At the time of the present invention it would have been obvious to one of ordinary skill in the art to modify the system of Kao by using it in an Ethernet controller device.

46. The motivation for doing so is taught by Cohen, in Col. 2, lines 6-28, namely that different devices that use a PCI bus use different configuration register settings. It may be possible to reuse the bus interface chip if the configuration settings are reprogrammable; therefore, the system to load the registers from a reprogrammable

memory is used. A further motivation is found in Bonaccio, which also teaches a similar system for loading configuration registers from an EEPROM. Bonaccio teaches in Par. 4 that using programmable registers is widely used in many ICs to allow the user to configure the function of the chip. Further, in Pars. 20-21, he teaches that the methods of loading configuration registers (which are similar to those of the present invention) may be applied not only to ICs such as hard disk channel controllers, but to any IC configured by registers.

47. Therefore, one of ordinary skill would be motivated to use the system of Kao in an Ethernet device as does Cohen, thereby obtaining the invention of claims 20-22.

***Conclusion***

All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse Diller whose telephone number is (571) 272-4173. The examiner can normally be reached on 9:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JD

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